WHAT IS CLAIMED IS:

1. A method of fabricating a CMOSFET comprising:

forming a plurality of gate patterns on a first region and a second region of a semiconductor substrate; then

forming gate spacers on both sidewalls of the gate patterns; then

forming a first impurity region of a first conductivity type in the first region of the semiconductor substrate; then

removing the gate spacers exposed at the first region; then

forming a second impurity region of the first conductivity type in the first region from which the gate spacers have been removed, the second impurity region having shallower depth than the first impurity region;

forming a third impurity region of a second conductivity type in the second region; then

removing the gate spacers exposed at the second region; and then

forming a fourth impurity region of the second conductivity type in the second region, the fourth impurity region having shallower depth than the third impurity region.

2. The method of fabricating the CMOSFET of claim 1,

wherein the first impurity region has higher impurity concentration than the second impurity region, and

wherein the third impurity region has higher impurity concentration than the fourth impurity region.

3. The method of fabricating the CMOSFET of claim 1,

wherein the first impurity region has higher impurity concentration than

the second impurity region, and

wherein the fourth impurity region has impurity concentration as high as the third impurity region.

4. The method of fabricating the CMOSFET of claim 1,

wherein the first impurity region is formed in the first region, using the gate pattern and the gate spacers as an ion implantation mask;

wherein the second impurity region is formed in the first region, using the gate pattern as an ion implantation mask;

wherein the third impurity region is formed in the second region, using the gate pattern and the gate spacers as an ion implantation mask; and

wherein the fourth region is formed in the second region, using the gate pattern as an ion implantation mask.

5. The method of fabricating the CMOSFET of the claim 1,

wherein the gate spacers comprise at least one selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, silicon carbide and silicon.

6. The method of fabricating the CMOSFET of claim 1,

wherein removing the gate spacers at the first region and second region are performed by isotropic etching.

7. The method of the CMOSFET of claim 1, wherein, before forming the third impurity region, a first HALO ion implantation is performed to form a first HALO region,

wherein the first HALO region is formed to cover sides of the first impurity region beneath the second impurity region.

8. The method of fabricating the CMOSFET of claim 1, wherein after

forming the fourth impurity region, a second HALO ion implantation is performed to form a second HALO region; and

wherein the second HALO region is formed to cover sides of the third impurity region beneath the fourth impurity region.

9. A method of fabricating a CMOSFET comprising the steps of:

forming a plurality of gate patterns on a first region and a second region of a semiconductor substrate; then

forming gate spacers on both sidewalls of the gate patterns; then

forming a first mask which covers the second region and exposes the first region; then

forming a first heavily doped region of a first conductivity type in the first region; then

removing the gate spacers which are exposed at the first region; then

forming a first lightly doped region of the first conductivity type in the first region; then

removing the first mask; then

forming a second mask which covers the first region and exposes the second region; then

forming a second heavily doped region of a second conductivity type in the second region; then

removing the gate spacers which are exposed at the second region; then

forming a second lightly doped region of the second conductivity type in the second region; and then

removing the second mask.

10. The method of fabricating the CMOSFET of claim 9, wherein the

first-conductivity-type is N-type.

11. The method of fabricating the CMOSFET of claim 9, wherein the second-conductivity-type is P-type.

12. The method of fabricating the CMOSFET of claim 9, wherein the forming of the first heavily doped region includes an ion implantation process which uses the first mask, the gate pattern and the gate spacer of the first region as an ion implantation mask; and

wherein the forming of the first lightly doped region includes an ion implantation process which uses the first mask and the gate pattern of the first region as an ion implantation mask.

13. The method of fabricating the CMOSFET of claim 9, wherein the forming of the second heavily doped region includes an ion implantation process which uses the second mask, the gate pattern and gate spacer of the second region as an implantation mask; and

wherein the forming of the second lightly doped region includes an ion implantation process which uses the second mask and gate pattern of the second region as an ion implantation mask.

14. The method of fabricating the CMOSFET of claim 9, wherein the first lightly doped region has shallower depth than the first heavily doped region, and

wherein the second lightly doped region has shallower depth than the second heavily doped region.

15. The method of fabricating the CMOSFET of claim 9, wherein the gate spacers comprise at least one selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, silicon carbide and silicon.

16. The method of fabricating the CMOSFET of claim 9, wherein the first and second masks are photoresist patterns which are formed using a photolithographic process.

17. The method of fabricating the CMOSFET of claim 9, wherein before removing the first mask, a first HALO ion implantation is performed to form a first HALO region;

wherein the first HALO ion implantation process uses the gate pattern of the first region and the first mask as an ion implantation mask; and

wherein the first HALO region is formed to cover sides of the first heavily doped region beneath the first lightly doped region.

18. The method as defined by claim 17, wherein the first HALO ion implantation process uses the impurities of the second conductivity type.

19. The method of fabricating the CMOSFET of claim 9, wherein before removing the second mask, a second HALO ion implantation process is performed to form a second HALO region;

wherein the second HALO ion implantation process uses the gate pattern of the second region and the second mask as an ion implantation mask; and

wherein the second HALO region is formed to cover sides of the second heavily doped region beneath the second lightly doped region.

20. The method of fabricating the CMOSFET of claim 19, wherein the second HALO ion implantation process uses impurities of first conductivity type.

21. A method of fabricating a CMOSFET comprising the steps of:

forming a plurality of gate patterns on a first region and a second region of a semiconductor substrate; then

forming gate spacers on both sidewalls of the gate patterns; then

forming a first mask which covers the second region and exposes the first region; then

forming a first heavily doped region of a first conductivity type in the first region; then

removing the gate spacers which are exposed at the first region; then

forming a second lightly doped region of the first conductivity type in the first region; then

removing the first mask; then

forming a second mask which covers the first region and exposes the second region; then

forming a third heavily doped region of a second conductivity type in the second region; then

removing the gate spacers which are exposed at the second region; then

forming a fourth lightly doped region of the second conductivity type in the second region; and then

removing the second mask.

22. The method of fabricating the CMOSFET of claim 21, wherein the first-conductivity-type is N-type.

23. The method of fabricating the CMOSFET of claim 21, wherein the second-conductivity-type is P-type.

24. The method of fabricating the CMOSFET of claim 21, wherein the first heavily doped region and the third heavily doped region are formed deeper than the second lightly doped region and the fourth heavily doped region, respectively.

25. The method of fabricating the CMOSFET of claim 21, wherein the fourth impurity region has impurity concentration a high as the third impurity region.

26. The method of fabricating the CMOSFET of claim 21,

wherein the first heavily impurity region is formed in the first region, using the gate pattern and the gate spacers as an ion implantation mask;

wherein the second lightly impurity region is formed in the first region, using the gate pattern as an ion implantation mask;

wherein the third heavily impurity region is formed in the second region, using the gate pattern and the gate spacers as an ion implantation mask; and

wherein the fourth heavily impurity region is formed in the second region, using the gate pattern as an ion implantation mask.

27. The method of fabricating the CMOSFET of claim 21,

wherein before forming the third heavily doped region, a first HALO ion implantation process is performed to form a first HALO region;

wherein the first HALO ion implantation process uses the gate pattern of the first region as an ion implantation mask; and

wherein the first HALO region is formed to cover sides of the first heavily doped region beneath the second lightly doped region.

28. The method as defined by claim 27, wherein the first HALO ion implantation process uses P-type impurity.

29. The method of fabricating the CMOSFET of claim 21,

wherein after forming the fourth heavily doped region, a second HALO ion implantation process is performed to form a second HALO ion region;

wherein the second HALO implantation region uses the gate pattern of the

second region as an ion implantation mask; and

wherein the second HALO region is formed to cover sides of the third high-concentration region beneath the fourth heavily doped region.

30. The method as defined by claim 29, wherein the second HALO ion implantation process uses N-type impurity.